IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1 and 11, and ADD new claim 15 in accordance with the following:

1. (currently amended) A semiconductor device comprising:

a plurality of function blocks;

a plurality of buses, each of which is respectively connected to one of the plurality of function blocks;

a plurality of control signal lines, which are separate from each other and are connected to the respective function blocks;

a main bus;

a bus control unit connected to the main bus; and

a bus division control unit located between the plurality of buses and the main bus, configured to couple one of the plurality of buses to the main bus and to transmit a control signal indicative of write operation or read operation to a corresponding one of the plurality of control signal lines in response to a decoded result of address information supplied from the bus control unit via the main bus, thereby controlling a corresponding one of the plurality of function blocks, wherein one control signal line is not connected to two or more function blocks.

2. (original) The semiconductor device as claimed in claim 1, wherein the bus division control unit comprises:

a decoder unit for decoding the information supplied from the bus control unit via the main bus and generating the control signal; and

a bus dividing unit for connecting one of the plurality of buses to the main bus, in accordance with a decoded result of the decoder unit.

3. (original) The semiconductor device as claimed in claim 1, wherein the bus division

control unit connects one of the plurality of buses to the main bus, in accordance with a decoded result of address information transmitted from the bus control unit via the main bus.

4. (original) The semiconductor device as claimed in claim 1, wherein

at least two of the plurality of function blocks shares one of the plurality of buses, and

the bus division control unit controls a transfer operation between the two function blocks via the one of the plurality of buses in response to a transfer request signal.

5. (original) The semiconductor device as claimed in claim 4, wherein the bus division control unit simultaneously transmits a write-enable signal to one of the two function blocks and a read-enable signal to the other one of the two function blocks.

6. (original) The semiconductor device as claimed in claim 4, wherein the bus division control unit receives a transfer control signal and determines a transfer source and a transfer destination between the two function blocks in accordance with the transfer control signal.

7. (original) The semiconductor device as claimed in claim 4, wherein, when an access request to one of the two function blocks is made by the bus control unit, the bus division control unit processes the access request prior to processing the transfer request.

8. (original) The semiconductor device as claimed in claim 4, wherein, when an access request to one of the plurality of function blocks other than the two function blocks is made by the bus control unit, the bus division control unit processes the access request in parallel with processing the transfer request.

9. (original) The semiconductor device as claimed in claim 1, wherein the bus division control unit determines whether an access made by the bus control unit is a read access or a write access based on a decoded result of information supplied from the bus control unit via the main bus, and connects one of the plurality of buses to the main bus in the access direction as determined based on the decoded result of information supplied from the bus control unit via the main bus.

10. (cancelled)

11. (currently amended) A semiconductor device comprising:

a plurality of function blocks;

a plurality of data buses, each connected to one of the plurality of function blocks;

a plurality of control signal lines, each connected to a corresponding one of the plurality of function blocks;

an address/data bus having a main control signal line;

a bus control unit connected to the address/data bus; and

a bus division control unit arranged to decode address information received from the bus control unit via the address/data bus, couple the address/data bus to the plurality of data buses, and transmit a control signal indicative of write operation or read operation from the main control signal line via one of the plurality of control signal lines to control the corresponding one of the plurality of function blocks, wherein one control signal line is not connected to two or more function blocks.

12-14. (cancelled)

15. (new) A semiconductor device comprising:

a plurality of function blocks;

a plurality of buses, each of which is respectively connected to one of the plurality of function blocks;

a plurality of control signal lines, each of which is respectively connected to one of the plurality of function blocks;

a main bus;

a bus control unit connected to the main bus; and

a bus division control unit located between the plurality of buses and the main bus, for connecting a first bus of the plurality of buses to the main bus in accordance with a decoded result of information on the main bus, and controlling a transferring operation between two function blocks connected to a vacant shared second bus of the plurality of buses, and wherein the two function blocks are selected without regard to access frequency.